CLAIMS

1. A computer-implemented method for use in a computer system comprising a plurality of logical devices coupled to a bus associated with a configuration space including a plurality of functions, the method comprising steps of:

(A) determining whether a compatibility flag indicates that each of the plurality of logical devices should be mapped to a distinct one of the plurality of functions;

(B) mapping each of the plurality of logical devices to a distinct one of the plurality of functions if it is determined in step (A) that the plurality of logical devices should be so mapped; and

(C) otherwise, mapping at least two of the plurality of logical devices to a single one of the plurality of functions.

2. The method of claim 1, wherein the bus comprises a Peripheral Component Interconnect (PCI) bus.

3. The method of claim 2, wherein the step (C) comprises a step of storing a value in a field of a PCI header associated with the single one of the plurality of functions in the configuration space, wherein the value indicates that multiple logical devices are mapped to the single one of the plurality of functions.

4. The method of claim 3, wherein the field comprises the subsystem ID field of the PCI header.

5. The method of claim 1, wherein the computer system further comprises a plurality of physical devices coupled to the bus, wherein each of the plurality of physical devices implements at least one of the plurality of logical devices, and wherein the step (C) comprises a step of:

(C)(1) for each physical device *D* in the plurality of physical devices:

(a) identifying a set *S* of logical devices implemented by physical device *D*; and

(b) mapping all of the logical devices in set *S* to a single function associated with the physical device *D*.

6. The method of claim 1, wherein the computer system further comprises a plurality of physical devices coupled to the bus, wherein each of the plurality of physical devices implements at least one of the plurality of logical devices, and wherein the step (B) comprises a step of:

(B)(1) for each physical device *D* in the plurality of physical devices:

(a) identifying a set *S* of logical devices implemented by physical device *D*; and

(b) mapping each of the logical devices in set *S* to a distinct function associated with the physical device *D*.

7. A computer-implemented method for use in a computer system including a plurality of physical devices coupled to a Peripheral Component Interconnect (PCI) bus associated with a configuration space including a plurality of functions, each of the plurality of physical devices implementing at least one of a plurality of logical devices coupled to the PCI bus, the method comprising steps of:

(A) determining whether a compatibility flag indicates that each of the plurality of logical devices should be mapped to a distinct one of the plurality of functions;

(B) if it is determined in step (A) that each of the plurality of logical devices should be mapped to a distinct one of the plurality of functions, then for each physical device *D* in the plurality of physical devices, performing steps of:

(1) identifying a set *S* of logical devices implemented by physical device *D*; and

(2) mapping each of the logical devices in set *S* to a distinct function associated with the physical device *D*;

(C) otherwise, for each physical device *D* in the plurality of physical devices, performing steps of:

(1) identifying a set *S* of logical devices implemented by physical device *D*; and

(2) mapping all of logical devices in set *S* to a single function in a portion of the configuration space associated with physical device *D* by storing a value in a subsystem ID field of a PCI header in the portion of the configuration space, wherein the value

indicates that multiple logical devices are mapped to the single function.

8. A device for use in a computer system including a plurality of logical devices coupled to a bus associated with a configuration space including a plurality of functions, the device comprising:

determination means for determining whether a compatibility flag indicates that each of the plurality of logical devices should be mapped to a distinct one of the plurality of functions;

first mapping means for mapping each of the plurality of logical devices to a distinct one of the plurality of functions if the determination means determines that the plurality of logical devices should be so mapped; and

second mapping means for mapping at least two of the plurality of logical devices to a single one of the plurality of functions if the determination means does not determine that each of the plurality of logical devices should be mapped to a distinct one of the plurality of functions.

9. The device of claim 8, wherein the bus comprises a Peripheral Component Interconnect (PCI) bus.

10. The device of claim 9, wherein the second mapping means comprises means for storing a value in a field of a PCI header associated with the single one of the plurality of functions in the configuration space, wherein the value indicates that multiple logical devices are mapped to the single one of the plurality of functions.

11. The device of claim 10, wherein the field comprises the subsystem ID field of the PCI header.

12. The device of claim 8, wherein the computer system further comprises a plurality of physical devices coupled to the bus, wherein each of the plurality of physical devices implements at least one of the plurality of logical devices, and wherein the second mapping means comprises means for: (1) identifying, for each physical device *D* in the plurality of physical devices, a set *S* of logical devices implemented by physical device *D*; and (2) mapping all of the logical devices in set *S* to a single function associated with the physical device *D*.

13. The device of claim 8, wherein the computer system further comprises a plurality of physical devices coupled to the bus, wherein each of the plurality of physical devices implements at least one of the plurality of logical devices, and wherein the first mapping means comprises means for: (1) identifying, for each physical device *D* in the plurality of physical devices, a set *S* of logical devices implemented by physical device *D*; and (2) mapping each of the logical devices in set *S* to a distinct function associated with the physical device *D*.

14. A computer-implemented method for use in a computer system comprising a plurality of logical devices coupled to a bus associated with a configuration space including a plurality of functions, the method comprising steps of:

(A) determining whether an operating system selected to be executed in the computer system supports mapping of multiple logical devices to a single function;

(B) mapping each of the plurality of logical devices to a distinct one of the plurality of functions if it is determined in step (A) that the operating system selected to be executed in the computer system does not support mapping of multiple logical devices to a single function; and

(C) otherwise, mapping at least two of the plurality of logical devices to a single one of the plurality of functions.

15. The method of claim 14, wherein the bus comprises a Peripheral Component Interconnect (PCI) bus.

16. The method of claim 15, wherein the step (C) comprises a step of storing a value in a field of a PCI header associated with the single one of the plurality of functions in the configuration space, wherein the value indicates that multiple logical devices are mapped to the single one of the plurality of functions.

17. The method of claim 16, wherein the field comprises the subsystem ID field of the PCI header.

18. The method of claim 14, wherein the computer system further comprises a plurality of physical devices coupled to the bus, wherein each of the plurality of physical devices implements at least one of the plurality of logical devices, and wherein the step (C) comprises a step of:

(C)(1) for each physical device *D* in the plurality of physical devices:

(c) identifying a set *S* of logical devices implemented by physical device *D*; and

(d) mapping all of the logical devices in set *S* to a single function associated with the physical device *D*.

19. The method of claim 14, wherein the computer system further comprises a plurality of physical devices coupled to the bus, wherein each of the plurality of physical devices implements at least one of the plurality of logical devices, and wherein the step (B) comprises a step of:

(B)(1) for each physical device *D* in the plurality of physical devices:

(a) identifying a set *S* of logical devices implemented by physical device *D*; and

(b) mapping each of the logical devices in set *S* to a separate function associated with the physical device *D*.

20. The method of claim 14, wherein the operating system comprises an HP-UX operating system.

21. The method of claim 14, wherein the operating system comprises a Microsoft .NET operating system.

22. The method of claim 14, wherein the computer system further comprises a plurality of operating systems including the operating system selected to be executed in the computer system.

23. A computer-implemented method for use in a computer system including a plurality of physical devices coupled to a Peripheral Component Interconnect (PCI) bus associated with a configuration space including a plurality of functions, each of the plurality of physical devices implementing at least one of a plurality of logical devices coupled to the bus, the method comprising steps of:

(A) determining whether an operating system selected to be executed in the computer system supports mapping of multiple logical devices to a single function;

(B) if it is determined in step (A) that the operating system selected to be executed in the computer system does not support mapping of multiple logical devices to a single function, then for each physical device *D* in the plurality of physical devices, performing steps of:

(1) identifying a first set *S* of logical devices implemented by physical device *D*; and

(2) mapping each of the logical devices in the first set *S* to a separate function associated with the physical device *D*; and

(C) otherwise, for each physical device *D* in the plurality of physical devices, performing steps of:

(1) identifying a second set *S* of logical devices implemented by physical device *D*; and

(2) mapping all of the logical devices in the second set *S* to a single function associated with the physical device *D*.

24. A device for use in a computer system including a plurality of logical devices coupled to a bus associated with a configuration space including a plurality of functions, the device comprising:

determination means for determining whether an operating system selected to be executed in the computer system supports mapping of multiple logical devices to a single function;

first mapping means for mapping each of the plurality of logical devices to a distinct one of the plurality of functions if the determination means determines that the operating system selected to be executed in the computer system does not support mapping of multiple logical devices to a single function; and

second mapping means for mapping at least two of the plurality of logical devices to a single one of the plurality of functions if the determination means determines that the operating system selected to be executed in the computer supports mapping of multiple logical devices to a single function.

25. The device of claim 24, wherein the bus comprises a Peripheral Component Interconnect (PCI) bus.

26. The device of claim 25, wherein the second mapping means comprises means for storing a value in a field of a PCI header associated with the single one of the plurality of functions in the configuration space, wherein the value indicates that multiple logical devices are mapped to the single one of the plurality of functions.

27. The device of claim 26, wherein the field comprises the subsystem ID field of the PCI header.

28. The device of claim 24, wherein the computer system further comprises a plurality of physical devices coupled to the bus, wherein each of the plurality of physical devices implements at least one of the plurality of logical devices, and wherein the second mapping means comprises means for: (1) identifying, for each physical device *D* in the plurality of physical devices, a set *S* of logical devices implemented by physical device *D*; and (2) mapping all of the logical devices in set *S* to a single function associated with the physical device *D*.

29. The device of claim 24, wherein the computer system further comprises a plurality of physical devices coupled to the bus, wherein each of the plurality of physical devices implements at least one of the plurality of logical devices, and wherein the first mapping means comprises means for: (1) identifying, for each physical device *D* in the plurality of physical devices, a set *S* of logical devices implemented by physical device *D*; and (2) mapping each of the logical devices in set *S* to a separate function associated with the physical device *D*.

30. The device of claim 24, wherein the operating system comprises an HP-UX operating system.

31. The device of claim 24, wherein the operating system comprises a Microsoft .NET operating system.

32. The device of claim 24, wherein the computer system further comprises a plurality of operating systems including the operating system selected to be executed in the computer system.